WHAT IS CLAIMED IS:

1. A delay producing method using first-stage to N^{th}-stage delay elements connected in series to each other and, when a clock signal is inputted to an input side of said first-stage delay element, producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element, said delay producing method comprising:

using first-stage and second-stage to N^{th}-stage selectors arranged in one-to-one correspondence with said delay elements, and each outputting one selected from two inputs;

using, as one of inputs to each of said first-stage to N^{th}-stage selectors, an input to a corresponding one of said delay elements;

using, as the other of the inputs to each of said first-stage to $(N-1)^{th}$-stage selectors, an output from said selector of the next but one stage;

outputting said even-stage delayed signal from said first-stage selector; and

outputting said odd-stage delayed signal from said second-stage selector.

2. The delay producing method according to claim 1, wherein delay amounts of said first-stage to N^{th}-stage delay elements are equal to each other.

3. The delay producing method according to claim 1, wherein said first-stage to N^{th}-stage delay elements have different delay amounts.

4. A delay adjusting method based on said delay producing method according to claim 1, comprising the steps of synthesizing said even-stage delayed clock signal and said odd-stage delayed clock signal with each other and applying a fine adjustment thereto to thereby produce and output an internal clock signal.

5. A delay producing circuit including first-stage to N^{th}-stag delay

lements connected in s ri s to each other and, when a clock signal is inputted to an input side of said first-stage delay element, producing an even-stage delayed signal from a clock signal obtained from the even-stage delay element, and an odd-stage delayed signal from a clock signal obtained from the odd-stage delay element, said delay producing circuit comprising:

first-stage and second-stage to N^{th}-stage selectors arranged in one-to-one correspondence with said delay elements, and each having two input terminals and one output terminal,

wherein one of the input terminals of each of said first-stage to N^{th}-stage selectors is connected to an input side of a corresponding one of said delay elements, the other of the input terminals of each of said first-stage to $(N-1)^{th}$-stage selectors is connected to the output terminal of said selector of the next but one stage, said even-stage delayed signal is outputted from the output terminal of said first-stage selector, and said odd-stage delayed signal is outputted from the output terminal of said second-stage selector.

6. The delay producing circuit according to claim 5, wherein delay amounts of said first-stage to N^{th}-stage delay elements are equal to each other.

7. The delay producing circuit according to claim 5, wherein said first-stage to N^{th}-stage delay elements have different delay amounts.

8. A delay adjusting circuit using said delay producing circuit according to claim 5, comprising a delay fine adjusting circuit that synthesizes said even-stage delayed clock signal and said odd-stage delayed clock signal with each other and applies a fine adjustment thereto to thereby produce and output an internal clock signal.

9. A delay producing circuit comprising N-stage delay elements connected in series to each other, and selectors that, in the state where a clock signal is inputted to an input side of the first-stage delay element, switchingly select delays of the given delay elements from input/output portions of said N-stage delay elements in response to a switching control signal from an

external control circuit, thereby to output an even-stage delayed clock signal and an odd-stage delayed clock signal,

wherein said selectors are 2:1 selectors each of the type that selectively outputs one from two inputs, and include for-even-stage selectors connected in series to each other so as to successively receive, as one input sequence, an output from the input side of said first-stage delay element, and outputs from output sides of the second-stage to $(N-1)^{th}$-stage delay elements, said outputs each received from every other one of said input/output portions of said N-stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable said even-stage delayed clock signal obtained by the selector of the stage switchingly selected by said switching control signal, to be outputted through the first-stage selector, and further include for-odd-stage selectors connected in series to each other so as to successively receive, as one input sequence, an output from an output side of said first-stage delay element, and outputs from output sides of the third-stage to N^{th}-stage delay elements, said outputs each received from every other one of said input/output portions of said N-stage delay elements, and further receive, as the other input sequence, outputs from the second-stage and subsequent selectors at the prior-stage selectors, respectively, thereby to enable said odd-stage delayed clock signal obtained by the selector of the stage switchingly selected by said switching control signal, to be outputted through the first-stage selector.